

Advances in Semiconductor Materials 2025–2026

What Is Technically Real—and What Matters for Implementation

Technical whitepaper

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High-tech advisory for process implementation, stability and defect reduction.

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Abstract

Semiconductor manufacturing continues to advance through scaling, new materials, tighter process control and increasingly complex integration. This whitepaper examines five developments that crossed important implementation thresholds during 2025–2026: high-NA EUV patterning materials, fine-pitch hybrid-bonding interfaces, molybdenum word-line metallization in 3D NAND, glass-core packaging substrates, and PFAS- and fluorine-free ArF immersion resists. The evidence spans advanced pilot-line demonstrations, customer evaluation and sampling, and selected high-volume production. Across the five cases, intrinsic material performance is only the starting point. Manufacturing value depends on whether that advantage survives the surrounding integration flow, qualification requirements and production-scale process control. The 2025–2026 developments therefore broaden the technical toolbox without implying universal replacement of incumbent materials. Production adoption remains selective and application-specific, with the strongest cases emerging where a measurable technical advantage is paired with sufficiently controlled integration burden.

Introduction

Semiconductor manufacturing has always advanced through scaling, new materials, tighter process control and increasingly complex integration [1]. What is notable since early 2025 is not a new development model, but the number of material and process concepts crossing important implementation thresholds. Some are moving from research and pilot lines toward qualification; others have entered selective production without becoming universal solutions.

The relevant question is therefore rarely which material is intrinsically “best.” What matters in manufacturing is whether that advantage can be preserved once the material is embedded in the complete production environment and subjected to the qualification, control and reliability demands of a fab. New materials may also require different equipment capabilities or infrastructure. A technical advantage becomes a production advantage only when the resulting material–process system can be operated robustly at manufacturing scale.

This whitepaper examines five 2025–2026 developments: high-NA EUV patterning materials; fine-pitch hybrid-bonding materials and interface chemistry; molybdenum word-line metallization in 3D NAND; glass-core packaging substrates; and PFAS- and fluorine-free ArF immersion resists. They were selected to cover distinct material roles—patterning, bonding interfaces, metallization, substrates and formulation redesign—across lithography, memory and advanced packaging.

The five cases also span very different maturity levels. A laboratory or pilot-line result can establish technical feasibility, but manufacturing relevance depends on repeatability, defect control, qualification and production adoption. The discussion therefore distinguishes technical demonstration from manufacturing readiness. Equipment and process developments are included only where they enable, constrain or demonstrate implementation of the material change; they are not treated as independent technology advances in this materials-focused review. Maturity assessments are based on dated public evidence through July 2026.

Taken together, the cases provide a practical view of how semiconductor materials move from promising options toward durable production platforms: the decisive question is where the demonstrated benefit is large enough, and the integration burden sufficiently controlled, to justify

implementation. The first case—high-NA EUV patterning—shows this particularly well, as progress increasingly depends not on resist performance alone, but on the interaction of the complete patterning stack.

Five semiconductor developments at a glance

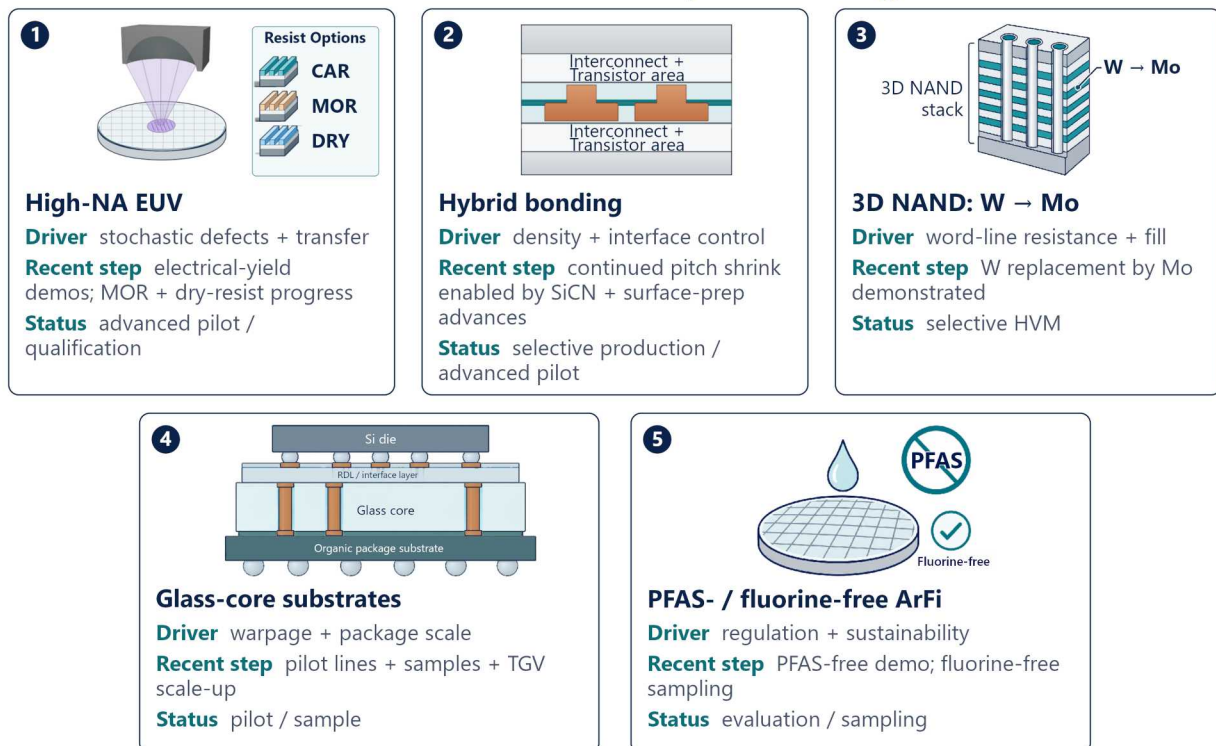


Figure 1. Five semiconductor developments at a glance: high-NA EUV patterning, hybrid bonding, 3D NAND W → Mo, glass-core substrates, and PFAS-/fluorine-free ArFi.

Source: ProcessRoute Advisory synthesis based on refs. 2–27.

1) High-NA EUV patterning: from resist performance to a distributed error budget

1.1 EUV resist platforms mature and diversify

Chemically amplified resist (CAR) remains the established EUV manufacturing platform. It has the deepest formulation, track, supply and qualification infrastructure, together with the largest body of manufacturing experience. Continued development has extended CAR performance as EUV dimensions have scaled, but the materials challenge becomes increasingly demanding as feature dimensions and resist films shrink. Stochastic variation has to be controlled while sufficient imaging contrast, mechanical stability and etch resistance are retained for reliable pattern transfer. CAR is therefore not being displaced by a single superior material; rather, increasingly aggressive patterning has created room for alternative resist architectures.

Metal-oxide resist (MOR) and deposited dry resist are the most prominent alternatives. MOR currently provides some of the strongest public wet-applied results at aggressive high-NA pitches, while dry resist has emerged as a third credible platform alongside CAR and MOR. Neither eliminates the fundamental challenges of stochastic patterning, and neither has replaced CAR as

the manufacturing baseline. Their significance is that they provide additional ways of balancing the competing requirements of increasingly thin resist films and smaller feature dimensions.

During 2025–2026, these alternatives moved beyond materials screening toward increasingly integrated demonstrations. In January 2025, Lam reported that its dry-resist technology had been qualified by imec for 28 nm-pitch direct-print back-end-of-line (BEOL) logic using 0.33-NA EUV.[2] Subsequent high-NA work demonstrated 18 nm-pitch dense lines and spaces with a quantified defect-free window after co-optimizing the resist, underlayer, post-exposure bake and dry development.[3] MOR meanwhile underpinned some of the most aggressive high-NA patterning results reported during the same period. The question is therefore increasingly no longer simply whether a resist can resolve the required feature, but how reliably that pattern can be transferred into a functional structure.

1.2 From pattern quality to electrical functionality

Electrical performance has always been the ultimate qualification target, but it can only be assessed after successful pattern formation and transfer. For an established resist and process flow, substantial experience exists linking pattern metrics and defect signatures to downstream electrical behavior. With a newer resist platform, that relationship first has to be established. Apparently good imaging or pattern-transfer results therefore do not by themselves demonstrate that the resulting structures will deliver acceptable electrical yield.

Public results since early 2025 have begun to provide this evidence. In February 2025, imec reported more than 90% electrical yield on 20 nm metal-pitch test structures patterned by single-exposure high-NA EUV using a negative-tone MOR and transferred through the hard-mask flow.[4] In September 2025, imec reported 13 nm tip-to-tip structures at 20 nm pitch together with functional 20 nm- and 18 nm-pitch ruthenium (Ru) direct-metal-etch structures; the disclosed 20 nm-pitch direct metal etch (DME) vehicle reached 100% electrical test yield.[5] In July 2026, Lam, ASML and imec also reported a 20 nm-pitch Ru interconnect yield demonstration using the Aether dry-resist platform.[6]

These remain advanced research and pilot-line vehicles rather than broad product qualification, but they move the evidence beyond attractive resist images or isolated patterning metrics. They show that patterns produced with newer resist platforms can survive transfer into electrically functional structures at dimensions relevant to high-NA EUV.

Establishing that link also requires more than conventional pattern averages. Critical dimension (CD), local critical-dimension uniformity (LCDU) and roughness remain important, but they do not fully capture the rare stochastic failures that can ultimately limit yield. Imec's use of electron-beam (e-beam) defect inspection together with serpentine and fork-fork electrical structures helps correlate pattern defects with subsequent opens and shorts.[4,5] High-resolution inspection, after-etch metrology and electrical test therefore form complementary parts of the qualification and learning loop.

1.3 Manufacturing implications: a more distributed error budget

The progress of the resist platforms changes the relative importance of the different contributors to EUV patterning performance. Resist stochasticity remains important, but continued improvement of EUV resist technology means that the resist is no longer usefully treated as the single dominant contributor. Mask and aerial-image quality, film thickness and underlayer behavior, development,

pattern transfer, cleaning and inspection increasingly consume significant parts of the same manufacturing margin.[3,5,7]

High-NA does not create this shift, but its tighter process margins make the interaction between these contributors still more consequential. Thinner imaging films increase the importance of underlayers for adhesion, surface energy, profile control and transfer selectivity. Aggressive MOR and dry-resist results have both required explicit resist/underlayer optimization.[3,5] The extension of MOR industrialization into precursor synthesis, filtration and chemical delivery further shows that control increasingly extends beyond the resist formulation itself and into the surrounding manufacturing infrastructure.[7]

In this respect, the EUV patterning ecosystem is beginning to resemble mature DUV lithography more closely. The underlying physics and the relative magnitude of individual contributors are not the same, but as EUV resist platforms mature, manufacturing performance increasingly depends on controlling several significant contributors rather than overcoming one overwhelmingly dominant materials limitation.

The strongest 2025–2026 evidence is therefore not simply that high-NA EUV can print a 20 nm-class pitch. It is that these patterns can increasingly be transferred into electrically testable structures at high reported yield on advanced research vehicles. MOR and dry resist have strengthened their industrial cases while CAR remains the incumbent platform. The next decisive threshold is broader customer product-layer qualification with repeatable multi-lot defect and electrical-yield data.

2) Fine-pitch hybrid bonding: the material stack evolves as the interface window shrinks

2.1 Why fine-pitch scaling makes the interface critical

Hybrid bonding forms dielectric and metal interfaces directly, without the solder bump used in conventional microbump approaches. The dielectric surfaces establish the initial mechanical bond, while copper (Cu) pads form the electrical connection during anneal. Removing the solder enables much smaller interconnect pitch, but makes electrical yield increasingly dependent on nanometer-scale surface condition and topography.

Recent demonstrations show how far this has progressed. In May 2026, imec and EV Group (EVG) demonstrated wafer-to-wafer (W2W) bonding at 200 nm Cu-pad pitch with a post-bond overlay vector below 40 nm for all dies across a 300 mm wafer.[8] At these dimensions, reduced pad overlap can produce high resistance or opens and jeopardize dies that were electrically good before stacking. TSMC also states that its 3 nm System on Integrated Chips (SoIC) stacking technology entered volume production in 2025,[9]¹ although the most aggressive sub-micrometer demonstrations remain test-vehicle evidence. The materials question is therefore increasingly central: what changes in the bonding stack are needed to make such pitches manufacturable?

¹ In TSMC's SoIC statement, '3 nm' refers to the semiconductor process generation of the stacked dies, not to the bonding pitch; TSMC separately states that SoIC bond-pitch scaling starts in the sub-10 μm regime.[9]

2.2 The bonding stack changes: SiCN, self-formed MnO_x and engineered surface chemistry

The first important material is **SiCN (silicon carbonitride) as the bonding dielectric**. SiCN itself is not new; the development is its increasing implementation in aggressively scaled Cu/SiCN hybrid bonding. In imec's 200 nm W2W demonstration, SiCN was identified as a critical element of the flow: the dielectric surface was planarized by chemical mechanical planarization (CMP) while the Cu pads were held at a recess of only a few nanometers.[8] SiCN is therefore part of the actual bonding interface and must combine flatness, chemical activatability and mechanical robustness with Cu compatibility.

A second development is the **self-formed MnO_x (manganese oxide) barrier derived from a Cu–Mn (copper–manganese) alloy seed**. At the 2025 IEEE Electronic Components and Technology Conference (ECTC), imec demonstrated this scheme in a 400 nm-pitch W2W process with high electrical yield on large daisy chains and evaluated dielectric breakdown, Cu diffusion, Cu bulge-out and electromigration.[10] The concept itself is not new: Mn-based self-forming barriers have a longer research history in scaled Cu BEOL interconnects.[11] The 2025 result transfers that concept into fine-pitch hybrid bonding, where the main value is barrier integrity and reliability at the bonding pad while preserving the tightly controlled Cu/dielectric interface.

The third development is **deliberate engineering of the dielectric surface state through plasma chemistry**. A 2026 SiCN study found that optimized N₂ (nitrogen) plasma generated nitrogen- and carbon-containing reactive groups and produced the highest bond strength, whereas O₂ (oxygen) plasma created a more uniform, hydroxyl-rich SiO₂ (silicon dioxide)-like surface with lower post-bond distortion but lower maximum strength.[12] That study covered dielectric-to-dielectric bonding, not exposed Cu. A separate 2025 Cu/SiO₂ study showed the relevant Cu constraint: O₂ plasma improves hydrophilicity but promotes Cu oxidation, while N₂ provides a more suitable compromise.[13] Plasma chemistry therefore creates a different interfacial material state even though the plasma gas itself is not a new structural material.

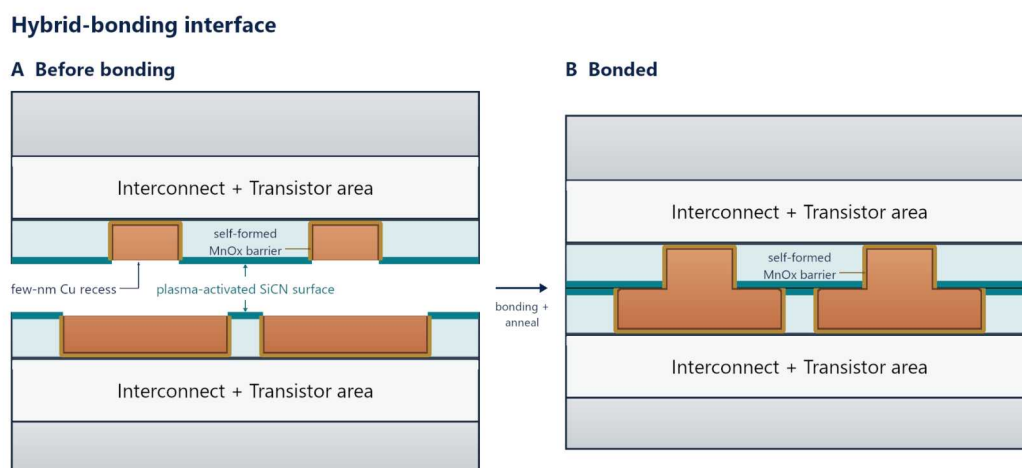


Figure 2. Fine-pitch hybrid-bonding interface: Cu pads, SiCN bonding dielectric, self-formed MnO_x barrier concept and activated bonding surface.

Source: ProcessRoute Advisory schematic based on refs. 8, 10, 12–14. Individual interface elements shown were demonstrated in separate fine-pitch hybrid-bonding studies; the schematic does not imply one production-qualified stack. Schematic, not to scale.

2.3 Manufacturing consequence: interface preparation becomes a coupled process sequence

The material stack described above has to be brought into a very narrow geometrical and chemical condition before bonding. Unlike conventional microbump structures, where the solder joint can accommodate larger variations in pillar height, Cu/dielectric hybrid bonding requires the Cu pads to remain only a few nanometers below the dielectric surface. The recess must be large enough for the dielectric surfaces to establish the initial bond, but small enough for Cu expansion during anneal to close the remaining gap and form a reliable electrical contact.[8,14] The manufacturing requirement is therefore not simply a target recess value, but a tightly controlled and sufficiently uniform recess distribution across the wafer.

Achieving that condition couples CMP directly to the subsequent wet processing. CMP establishes the initial Cu/dielectric topography, while post-CMP cleaning—and, depending on the integration flow, additional wet recessing—can further modify the Cu height. These steps therefore have to be developed together so that the required recess is reached uniformly across the wafer while residues, particles and surface contamination are removed. A 2025 study on fine-pitch hybrid bonding reported an acceptable Cu recess of about 3 nm and showed that post-CMP wet cleaning can materially affect the resulting recess.[14] At this scale, the wet step is therefore part of the topography-control process rather than merely a cleaning operation.

Once the required topography has been established, the bonding surfaces still require final preparation before bonding. Plasma activation is one established option, but more generally the surface-treatment step has to create the required dielectric surface state while remaining compatible with the exposed Cu and any additional materials in the stack. The N₂- and O₂-plasma studies discussed in Section 2.2 illustrate this constraint: treatments that improve dielectric activation can also alter the Cu surface, so the final surface-preparation process cannot be selected independently of the material system.[12,13] The same principle applies to newer stack elements such as Cu–Mn-derived MnO_x: their introduction expands the set of materials with which CMP, wet processing and final surface preparation must remain compatible.

The maturity of these elements remains unequal. Cu/SiCN bonding has been demonstrated at 200 nm W2W pitch,[8] while the Cu–Mn-derived MnO_x barrier has been demonstrated at 400 nm with high electrical yield.[10] Detailed SiCN plasma-chemistry studies remain at research level.[12] The available evidence therefore does not yet establish these developments as one production-qualified material stack. The next manufacturing threshold is repeatable control of interface topography, surface chemistry, contamination and electrical reliability across production wafers and lots.

3) 3D NAND word lines: molybdenum enters production as tungsten scaling limits tighten

3.1 Why tungsten becomes increasingly difficult to scale

In 3D NAND, word lines form repeated metal gate structures through an increasingly tall vertical stack. Continued density scaling therefore raises pressure on the resistance, fill behavior and material budget of each word line, driving selected advanced NAND flows from tungsten (W) toward molybdenum (Mo).

W integration becomes less favorable as conductor dimensions shrink because effective resistance depends not only on the metal itself but also on the fraction occupied by adhesion and barrier layers. Lam Research's 2025 ALTUS Halo disclosure states that Mo has lower nanoscale resistivity than W and can eliminate the conventional adhesion/barrier layer in the cited integration, with more than 50% resistance improvement over conventional W metallization in most instances.[15] The exact benefit is structure- and process-dependent, but removing liner volume becomes increasingly valuable as the word-line cross-section contracts.

Fill behavior adds a second advantage. As narrow cavities fill inward from their surfaces, the opening can pinch off before the cavity is complete, leaving voids or slit-like defects. Kioxia and Western Digital report that continued horizontal and vertical scaling makes W embedding increasingly difficult,[16] while Lam describes its Mo atomic layer deposition (ALD) process as providing improved fill and void-free metallization.[15] This is not an intrinsic “seam-free” property of Mo — Kioxia also shows that poorly optimized Mo can leave voids — but an integration advantage of an optimized Mo process at dimensions where W becomes increasingly difficult.

A further advantage concerns precursor chemistry. Conventional W deposition commonly uses WF_6 (tungsten hexafluoride). Kioxia and Western Digital report that fluorine retained in W voids or slits can migrate into surrounding dielectric regions and contribute to leakage and reliability degradation. Their Mo process instead uses fluorine-free MoO_2Cl_2 (molybdenum oxychloride), removing this specific fluorine reservoir and migration path while retaining the electrical advantages of Mo.[16] It also reduces reliance on fluorinated precursor chemistry, although the available evidence does not establish a comparative lifecycle environmental benefit.

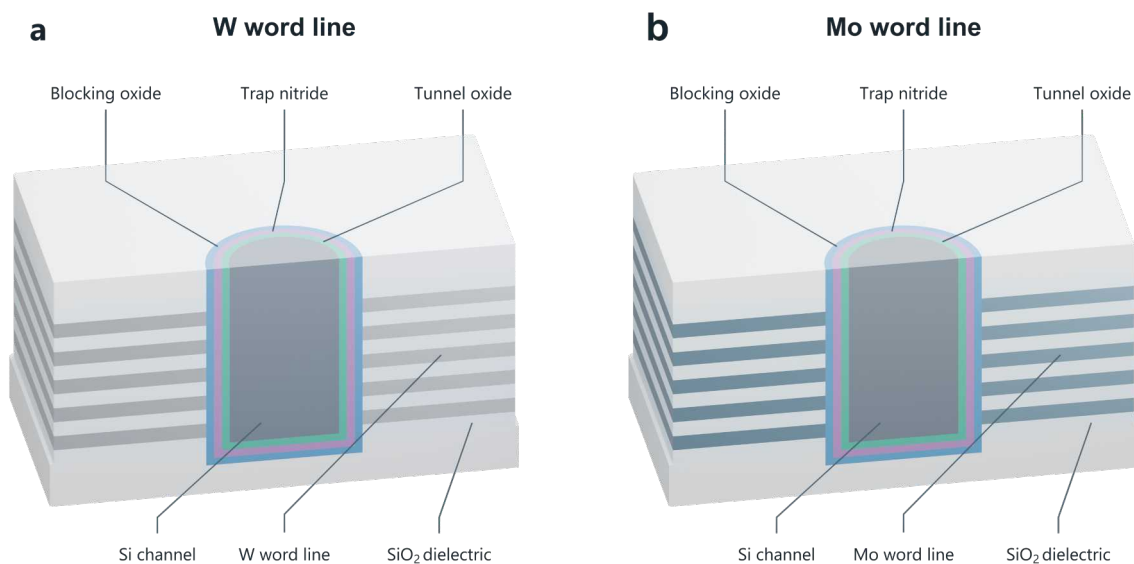


Figure 3. Simplified 3D NAND word-line comparison showing the transition from W to Mo within the repeated gate stack. Source: ProcessRoute Advisory schematic based on refs. 15–17. Schematic, not to scale.

3.2 From alternative metal to selective high-volume production

What changed in 2025–2026 is the maturity of the evidence. In February 2025, Lam introduced ALTUS Halo and quoted Micron as having brought Mo into mass production in its latest-generation NAND; Lam also reported early high-volume manufacturing (HVM) adoption at leading

3D NAND manufacturers in Korea and Singapore.[15] Mo has therefore moved beyond a materials comparison into selected production insertion.

The transition is not universal. Public evidence does not establish industry-wide replacement of W or convergence on one Mo integration scheme. Applied Materials' June 2026 disclosure nevertheless reinforces the production case by stating that low-resistance metals such as Mo are being adopted for NAND word-line metallization and linking the change to new process requirements in increasingly tall high-aspect-ratio structures.[17]

3.3 A metal substitution changes the surrounding integration flow

Mo is not a drop-in replacement for W. Kioxia's fluorine-free process illustrates one material-specific challenge: when Mo embeddability is poor, residual oxygen derived from MoO_2Cl_2 can accumulate in remaining voids. Kioxia reports that higher residual oxygen correlates with a higher leakage-failure rate and proposes that oxygen diffusing from these voids into cell and inter-word-line dielectrics forms leakage-current paths.[16] Fill quality therefore matters for dielectric reliability as well as geometry.

Manufacturing-scale Mo ALD also changes precursor delivery and thermal/process requirements. Lam identifies elevated-temperature capability, tight wafer-temperature control, advanced reactor/process sequencing and reliable bulk delivery of a **solid Mo precursor** as production requirements.[15] The removal of the conventional W adhesion/barrier layer simplifies one part of the stack, but Mo introduces its own chemical-handling and process-control requirements that must be qualified at production throughput.

Word-line separation itself is not new to Mo; W-based NAND also requires selective metal recess/separation after gate replacement. The new challenge is the combination of **Mo chemistry and increasingly tall stacks**. Applied Materials reports that conventional wet separation becomes progressively non-uniform because liquid chemistry struggles to reach the full depth of high-aspect-ratio structures, producing a top-heavy profile. Its Mo-selective dry removal process is intended to improve top-to-bottom uniformity and profile precision through the stack; Applied states that the process has been validated in HVM and links the improved uniformity to lower cell-to-cell variability, reduced leakage and improved data retention.[17]

The production transition therefore changes more than the conductor: it affects precursor logistics, deposition conditions, liner architecture, fill-defect and impurity control, selective removal and cleaning. The strongest public evidence by mid-2026 supports **selective HVM / production insertion**, while the breadth of adoption, comparative multi-lot yield and long-term reliability remain less visible. Mo has crossed the production threshold in selected advanced NAND, but broad industry-wide replacement of W is not yet established.

4) Glass-core substrates: a bridge between organic packaging and silicon interposers

4.1 Why glass occupies an intermediate materials space

Advanced packaging is currently anchored by two substrate classes. Organic substrates provide the lowest-cost and most mature large-format platform but face increasing warpage and dimensional-stability challenges as package size and routing density grow. Silicon interposers provide very high routing density, excellent dimensional stability and a close coefficient of thermal expansion (CTE)

match to silicon dies, but carry the cost, wafer-format and process complexity of a semiconductor-derived platform.

Glass occupies an intermediate materials space. Representative packaging glasses can achieve CTE values around 3.2–3.3 ppm/°C, close to silicon and substantially below typical organic core stacks.[18] Glass is also substantially stiffer and flatter than polymer-based substrates and offers the potential for large-panel processing rather than conventional silicon-wafer economics.[18,19] It is not a midpoint in every property—thermal conductivity remains far below silicon and electrical/mechanical behavior depends on composition and stack design—but its attraction lies in the **balance** of silicon-like dimensional stability with potentially more scalable package-format economics.

In that sense, glass can become both a literal and figurative bridge between organic package substrates and silicon interposers or dies. The practical question is whether this intermediate property set can be delivered at competitive yield and cost.

4.2 What has historically made glass difficult to industrialize

The barrier to glass adoption has not been attractive material properties, but turning a brittle, transparent material into a repeatable packaging platform. Through-glass vias (TGVs) need controlled geometry and sidewall quality, reliable metallization and thermal-cycle performance. Thin or large glass panels must survive handling, lithography, deposition, wet processing and assembly without excessive breakage or distortion, while inspection and metrology have to work across a substrate that behaves differently from both silicon wafers and organic panels.[19]

Transparency adds a specific integration burden. Wafer-handling, alignment and metrology systems developed around opaque silicon can rely on optical contrast or reflection; with glass, detection and alignment functions can require modified optics, sensors or recipes. Intel has described the broader transition as requiring the substrate industry to remap how it handles glass, while current alignment equipment often treats transparent alignment as a distinct operating mode.[20,21] These issues are increasingly engineered around, but they add equipment-compatibility and qualification work, particularly when older production tools are reused.

TGV formation is another manufacturing bottleneck. A via that is too tapered, rough or damaged can complicate metallization and reduce usable routing density. The industrial problem is therefore not simply whether holes can be made in glass, but whether large numbers of vias can be formed, cleaned, metallized, inspected and thermally cycled with sufficiently tight distributions for package-level yield.[22]

4.3 What changed in 2025–2026: from property argument to manufacturing evidence

The important change is that glass moved closer to a manufacturing threshold. DNP disclosed a pilot production line at Kuki, sample shipments beginning in early 2026, two glass-core substrate variants and a target to start mass production between April 2028 and March 2029.[23] That is not broad HVM adoption, but it moves the evidence beyond research coupons and roadmaps into pilot-line output and customer sampling.

AT&S described its glass-core work as moving from research toward industrial use, linking the platform to flatness, reduced electrical loss, finer structures, larger package formats and co-packaged optics.[19] Together with DNP's pilot-line evidence, this shows that glass is increasingly

being treated as a platform requiring an industrial supply chain rather than as an isolated materials experiment.

Process evidence also became more concrete. RENA demonstrated TGV processing on 510 × 515 mm glass and positioned alkaline glass etching as an alternative to hydrofluoric-acid (HF) processing.[22] The importance is not the equipment by itself, but what it demonstrates about the **glass material platform**: via formation and shaping are moving toward transferable processes suitable for customer tests and scale-up.

Table 1 — Advanced-packaging substrate platforms: complementary capabilities

Platform	Key advantage	Scale / dimensional behavior	Main implementation burden	2025–2026 maturity	Representative architectural fit
Organic / ABF substrate	Established ecosystem; cost-effective multilayer routing	Large formats established; warpage and dimensional stability become harder as package size and routing density grow	Layer build-up, warpage control, routing density, supply-chain constraints	Broad HVM baseline	Mainstream advanced packages where established infrastructure and cost matter
Glass-core substrate	High dimensional stability; engineerable CTE; attractive large-format potential	Attractive as package size grows; TGVs provide vertical connectivity	TGV formation / metallization, handling, inspection, reliability, new process qualification	Pilot / samples / industrialization	Large heterogeneous packages where dimensional stability and scale justify a new substrate platform
Silicon interposer	Highest routing precision; very fine interconnect capability	Excellent dimensional stability; economics and manufacturable area become increasingly important at large package size	Wafer processing, interposer cost, area scaling, integration complexity	Established HVM for selected high-end AI/HBM applications	AI/HBM and architectures requiring very high local interconnect density

Source: ProcessRoute Advisory synthesis based on refs. 18–23.

Glass broadens the advanced-packaging toolbox; it does not universally replace organic substrates or silicon interposers.

4.4 Where glass is likely to fit: co-integration rather than replacement

Glass is more likely to be **co-integrated with organic and silicon platforms than to replace either completely**. In a representative architecture, silicon dies or chiplets can interface through a glass-based interposer or core layer to an organic package substrate. Glass can therefore sit

physically between the silicon and organic parts of the package while providing a more stable intermediate routing platform.

Its strongest opportunity is where that intermediate property set adds value within a heterogeneous package: closer CTE matching and better dimensional stability on the silicon side, combined with the format and cost advantages of an organic package platform below. TGV yield, thin-glass handling, inspection, thermal reliability, ecosystem maturity and cost still have to be closed at production scale. If customer qualification and production-linked yield/reliability data continue to improve, glass may become both a **literal bridge in the package stack and a figurative bridge between the manufacturing economics of organic substrates and the performance of silicon interposers.**

5) PFAS- and fluorine-free ArF immersion resists: regulation becomes a materials-design constraint

5.1 Fluorinated functionality is embedded in ArF immersion performance

Argon-fluoride (ArF) immersion lithography is a mature and highly optimized platform, which makes material substitution unusually demanding. Fluorinated functionality has historically contributed both to resist chemistry and to the surface behavior required during immersion exposure. Hydrophobicity helps control interaction with the water interface and watermark-related defects, while the formulation still has to preserve the chemical response needed for imaging.[24]

The challenge is therefore not simply to remove a substance that may become more restricted. A replacement has to preserve the overall lithographic performance envelope: critical-dimension uniformity (CDU), line-width roughness (LWR), defectivity and stochastic failure behavior, dose and throughput, profile control, develop/rinse behavior, adhesion, pattern-transfer capability and etch resistance. Fluorinated functionality can affect surface energy, dissolution behavior and immersion-water compatibility, so its removal can require a genuine redesign of the resist formulation rather than a simple ingredient substitution.[24]

5.2 What changed in 2025–2026: PFAS-free first, fluorine-free next

In July 2025, Fujifilm and imec reported a negative-tone ArF immersion resist free of **per- and polyfluoroalkyl substances (PFAS)** under the cited definition. The material was demonstrated in a 28 nm-generation metal-wiring flow with high reported yield, and customer evaluations were underway.[24] This is integrated process evidence, not customer qualification or broad HVM replacement, but it establishes that PFAS-free chemistry has become technically credible in an ArF immersion flow.

A more aggressive milestone followed in April 2026, when Fujifilm announced a **fluorine-free negative-tone ArF immersion resist** and began customer sampling.[25] PFAS-free and fluorine-free are not interchangeable: the 2025 material removes materials within the cited PFAS definition, whereas the 2026 formulation goes further by eliminating fluorine from the resist design itself. By late July 2026, public evidence for the fluorine-free material was still at the sampling stage, with no independent customer qualification or comparative defect/yield dataset disclosed. **The technical question therefore shifts from whether such formulations can be made to whether they can reproduce the manufacturing performance expected from a highly mature ArF immersion resist platform.**

Table 2 — PFAS pressure and ArFi substitution status, 2025–2026

Development	2025–2026 evidence	Maturity	Remaining proof
PFAS-free negative ArFi	28 nm-generation metal-flow demo with imec; customer evaluation	integrated demo / evaluation	customer qualification; repeatable defect / yield data
Fluorine-free negative ArFi	customer sampling announced in 2026	customer sampling	customer qualification; comparative imaging, defectivity, stability

Source: ProcessRoute Advisory synthesis based on refs. 24–27. Maturity as of July 2026.

Substitution pressure is real — broad HVM replacement is not yet demonstrated.

5.3 Qualification means preserving the manufacturing performance envelope

A redesigned resist does not need to reproduce the exact focus, dose, bake or develop settings of the incumbent formulation; those parameters can be re-optimized. The relevant question is whether the resulting process still delivers the manufacturing performance required from ArF immersion lithography. That includes imaging at the target dimensions, critical-dimension uniformity (CDU), line-width roughness (LWR), rare bridges and breaks, profile control, develop/rinse behavior, pattern-transfer capability and throughput.

For immersion resists, the qualification burden extends beyond pattern formation itself. Removing fluorinated functionality can also change surface energy and the interaction between the resist and the immersion-water interface. Hydrophobic behavior, watermarks and immersion-related defectivity therefore have to be controlled alongside the conventional lithographic metrics. A formulation that prints an acceptable pattern but introduces water-interface or downstream defect problems would not constitute a manufacturing-equivalent replacement.

The 2025 imec result is important because the PFAS-free resist was demonstrated in an integrated 28 nm-generation metal-wiring flow with high reported yield and had entered customer evaluation. [24] That moves the evidence beyond isolated resist-pattern results, but it does not yet establish comparative multi-lot robustness or broad customer qualification. The 2026 fluorine-free formulation is one step earlier: customer sampling establishes that material is available for evaluation, but public evidence does not yet show comparable integrated defect and yield performance.[25] **The amount of qualification still required therefore increases with the depth of the chemistry change—and that matters because the regulatory timetable driving the change is itself still unresolved.**

5.4 Regulation becomes an engineering input before it becomes a final prohibition

The external driver here differs from the scaling-driven changes in the preceding sections. Regulatory and sustainability pressure is becoming part of the material-design specification. As of late July 2026, however, the European process had **not** resulted in a final blanket ban on semiconductor PFAS. The European Chemicals Agency (ECHA) published an updated universal-PFAS restriction proposal in August 2025, and by March 2026 the scientific evaluation had

progressed toward EU-wide restrictions with targeted **derogations** and emission controls, while the final European Commission decision was still pending.[26,27]

This unresolved regulatory timetable creates a difficult timing problem for both suppliers and semiconductor manufacturers. Material qualification and customer change-control can take years, so waiting for a final prohibition may leave insufficient time to develop, qualify and introduce an alternative without supply risk. Acting early, however, means investing in reformulation and qualification before the final regulatory scope, derogations and implementation dates are known. A chemistry that depends on compounds facing potential future restriction can therefore create long-term qualification, sourcing and change-control risk even while the exact regulatory outcome remains unsettled. The 2025–2026 shift is not that ArF immersion suddenly became non-compliant, but that mature resist chemistry is already being redesigned in anticipation of a different regulatory environment.

The central result is therefore a material one: PFAS-free ArF immersion resist has reached integrated demonstration and customer evaluation, while fluorine-free ArF immersion resist has reached customer sampling.[24,25] Neither has demonstrated broad HVM replacement, but regulatory pressure is already technically visible in the materials roadmap.

6) Conclusion: a wider technical toolbox, but a selective production toolbox

The five developments do not point to one dominant material transition. Instead, they show semiconductor manufacturing continuing to advance through several parallel routes, with materials and integration evolving alongside geometric scaling and, in some cases, in response to external constraints. The development pipeline therefore remains active; these changes continue to create new options for density, performance, power efficiency and manufacturability.

This broader development model is not new. Semiconductor progress has long combined geometric scaling with changes in device architecture, materials, integration and packaging. The 2025–2026 cases show that this model remains active, but also that each new option brings its own implementation and qualification burden.

The five cases also reinforce a long-established manufacturing principle: intrinsic material performance is only the starting point for industrial adoption. A material becomes valuable in production only when its advantage survives integration into a stable, controllable and economically viable manufacturing flow. Research and pilot lines may therefore widen the technical toolbox, while production remains selective and application-specific in how that toolbox is used.

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